EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	18350362	@ad<"19990922"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:50
L2	25555089	@ad<"20040211"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:50
L3	39916	"711"/$.CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:50
L4	36	(interleav$4 near2 bank$2) near6 simultaneous$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:50
L5	31	L2 and L4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:50
L6	22	L3 and L5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:50
L7	36714	((multiple or plural$4) or bank$4) and SRAM and DRAM	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:51
L8	5332	((multiple or plural$4) or bank$4) same SRAM same DRAM	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:51
L9	12845	DMA adj controller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:51

EAST Search History

L10	86221	(sufficient or enough) near2 (memory or space)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:51
L11	6860	(interleav$4 or non-interleav$4) same (simultaneous$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:53
L12	542	11 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:52
L13	347	2 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:52
L14	74	13 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:52
L15	25134	(interleav$4 or non-interleav$4).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:53
L16	7896	(interleav$4 or non-interleav$4).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:53
L17	19	14 and 15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:53
L18	11	14 and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/25 20:53

Terms used:
interleav and **bank** **near/6** **odd** or **even** and **simultaneous**

Found **16,414** of **215,186**

Sort results by: relevance
Display results: expanded form
Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next
Best 200 shown
Relevance scale

1 Poster Session 2: Odd/even bus invert with two-phase transfer for buses with coupling
Yan Zhang, John Lach, Kevin Skadron, Mircea R. Stan
August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design ISLPED '02**
Publisher: ACM Press
Full text available: pdf(239.83 KB) Additional Information: full citation, abstract, references, citings, index terms

The coupling capacitances between on-chip bus lines become dominant in deep-submicron technologies. Coding to reduce the *switching activity* of the individual lines was enough to reduce power on buses in older technologies, but new coding techniques that reduce the *coupling activity* between lines are needed for deep-submicron buses. One such coding technique uses the simple observation that coupling capacitances are always charged and discharged by activity on neighboring bus lines, ...

Keywords: bus invert, buses with coupling, coding for low-power I/O

2 Essays in computing science
C. A. R. Hoare
January 1989 Book
Publisher: Prentice-Hall, Inc.
Full text available: pdf(20.91 MB) Additional Information: full citation, abstract, references, cited by, review

Charles Antony Richard Hoare is one of the most productive and prolific computer scientists. This volume contains a selection of his published papers. There is a need, as in a Shakespearian Chorus, to offer some apology for what the book manifestly fails to achieve. It is not a complete 'collected works'. Selection between papers of this quality is not easy and, given the book's already considerable size, some difficult decisions as to what to omit have had to be made. Pity the editor weighin ...

3 Selected writings on computing: a personal perspective
Edsger W. Dijkstra
January 1982 Book
Publisher: Springer-Verlag New York, Inc.
Additional Information: full citation, abstract, references, cited by, index terms

Since the summer of 1973, when I became a Burroughs Research Fellow, my life has been very different from what it had been before. The daily routine changed: instead of going to the University each day, where I used to spend most of my time in the company of others, I now went there only one day a week and was most of the time that is, when not travelling!-- alone in my study. In my solitude, mail and the written word in general became more and more important. The circumstance that my employe ...

4 The security of all RSA and discrete log bits

Johan Håstad, Mats Näslund
March 2004 **Journal of the ACM (JACM)**, Volume 51 Issue 2
Publisher: ACM Press
Full text available: pdf(311.91 KB) Additional Information: full citation, abstract, references, index terms

We study the security of individual bits in an RSA encrypted message $E_N(x)$. We show that given $E_N(x)$, predicting any single bit in x with only a nonnegligible advantage over the trivial guessing strategy, is (through a polynomial-time reduction) as hard as breaking RSA. Moreover, we prove that blocks of $O(\log \log N)$ bits of x are computationally indistinguishable from random bits. The results carry over t ...

Keywords: Cryptography, RSA-encryption, bit-security, complexity, discrete logarithms

5 CMOS & logic applications optimization and techniques: Bus-encoding technique to reduce delay, power and simultaneous switching noise (SSN) in RLC interconnects

Chittarsu Raghunandan, K. S. Sainarayanan, M. B. Srinivas
March 2007 **Proceedings of the 17th great lakes symposium on Great lakes symposium on VLSI GLSVLSI '07**
Publisher: ACM Press
Full text available: pdf(325.04 KB) Additional Information: full citation, abstract, references, index terms

Inductance effects cannot be neglected in global interconnect lines as well as in circuits operating at higher frequencies. This paper presents a new spatio-temporal bus-encoding technique to minimize simultaneous switching noise as well as reduce delay and power dissipation in on-chip buses where inductance effects are dominating. Simulation experiments are carried out to find out the delay and SSN reduction for interconnect lines of different lengths (2mm, 5mm and 10mm) at various technology n ...

Keywords: bit transitions, bus-encoding scheme, crosstalk noise, decoder, delay, encoder, high impedance state, inductive coupling, low power, simultaneous switching noise (SSN), spatial and temporal redundancy

6 The theory of parsing, translation, and compiling

Alfred V. Aho, Jeffrey D. Ullman
January 1972 Book
Publisher: Prentice-Hall, Inc.
Full text available: pdf(98.28 MB) Additional Information: full citation, abstract, references, cited by, index terms

From volume 1 Preface (See Front Matter for full Preface)

This book is intended for a one or two semester course in compiling theory at the senior or graduate level. It is a theoretically oriented treatment of a practical subject. Our motivation for making it so is threefold.

(1) In an area as rapidly changing as Computer Science, sound pedagogy demands that

courses emphasize ideas, rather than implementation details. It is our hope that the algorithms and concepts presen ...

7 A taxonomy of parallel sorting

Dina Bitton, David J. DeWitt, David K. Hsaio, Jaishankar Menon
September 1984 **ACM Computing Surveys (CSUR)**, Volume 16 Issue 3
Publisher: ACM Press

Full text available: pdf(2.58 MB) Additional Information: full citation, references, citings, index terms, review

8 IBM system/360 principles of operation

IBM
January 1964 Book
Publisher: IBM Press
Full text available: pdf(14.82 MB) Additional Information: full citation, abstract, index terms

This manual is a comprehensive presentation of the eharaeteristies, functions, and features of the IBM System/ 360. The material is presented in a direct manner, assuming that the reader has a basic knowledge of IBM data processing systems and has read the IBM System/360 Systems Summary, Form A22-6810. The manual is useful for individual study, as an instruction aid, and as a machine reference manual.

The manual defines System/360 operating principles, central processing unit, instruct ...

9 GPGPU: general purpose computation on graphics hardware

David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn
August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**
Publisher: ACM Press
Full text available: pdf(63.03 MB) Additional Information: full citation, abstract, citings

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flexible processor. The latest graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully programmable vertex and pixel processing units that support vector operations up to full IEEE floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

10 Computation: finite and infinite machines

Marvin L. Minsky
January 1967 Book
Publisher: Prentice-Hall, Inc.
Additional Information: full citation, abstract, references, cited by, index terms

From the Preface (See Front Matter for full Preface)

Man has within a single generation found himself sharing the world with a strange new species: the computers and computer-like machines. Neither history, nor philosophy, nor common sense will tell us how these machines will affect us, for they do not do "work" as did machines of the Industrial Revolution. Instead of dealing with materials or energy, we are told that they handle "control" and "information" and even "intellectua ...

11 Session 8B: Holographic algorithms: from art to science

Jin-Yi Cai, Pinyan Lu
June 2007 **Proceedings of the thirty-ninth annual ACM symposium on Theory of computing STOC '07**
Publisher: ACM Press
Full text available: pdf(282.02 KB) Additional Information: full citation, abstract, references, index terms

We develop the theory of holographic algorithms. We definea basis manifold and give characterizations of algebraic varieties of realizable symmetric generators and recognizers on this manifold. We present a polynomial time decision algorithm for the simultaneous realizability problem. Using the general machinery we are able to giveunexpected holographic algorithms for some counting problems, modulo certain Mersenne type integers. These counting problems are P-complete without the moduli. Goin ...

Keywords: holographic algorithms, matchgates, signatures

12 Ultracomputers
Jacob T. Schwartz
October 1980 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 2 Issue 4
Publisher: ACM Press
Full text available: pdf(2.54 MB) Additional Information: full citation, abstract, references, citings, index terms

A class of parallel processors potentially involving thousands of individual processing elements is described. The architecture is based on the perfect shuffle connection and has two favorable characteristics: (1) Each processor communicates with a fixed number of other processors. (2) Important communication functions can be accomplished in time proportional to the logarithm of the number of processors. A number of basic algorithms for these "ultracomputers" are presented, and ...

13 Impact of interference on multi-hop wireless network performance
Kamal Jain, Jitendra Padhye, Venkata N. Padmanabhan, Lili Qiu
July 2005 **Wireless Networks**, Volume 11 Issue 4
Publisher: Kluwer Academic Publishers
Full text available: pdf(1.08 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we address the following question: given a specific placement of wireless nodes in physical space and a specific traffic workload, what is the maximum throughput that can be supported by the resulting network? Unlike previous work that has focused on computing asymptotic performance bounds under assumptions of homogeneity or randomness in the network topology and/or workload, we work with any given network and workload specified as inputs.A key issue impacting performance is wirel ...

14 On the scalability of cooperative time synchronization in pulse-connected networks
An-Swol Hu, Sergio D. Servetto
June 2006 **IEEE/ACM Transactions on Networking (TON)**, Volume 14 Issue SI
Publisher: IEEE Press
Full text available: pdf(624.47 KB) Additional Information: full citation, abstract, references, index terms

The problem of time synchronization in dense wireless networks is considered. Well-established synchronization techniques suffer from an inherent scalability problem in that synchronization errors grow with an increasing number of hops across the network. In this work, a model for communication in wireless networks is first developed, and then the model is used to define a new time synchronization mechanism. A salient feature of the proposed method is that, in the regime of asymptotically dense ...

Keywords: cooperation in networks, large network asymptotics, relay networks, scalability, sensor networks, time synchronization, wireless communications

15 Computing on an anonymous ring

Hagit Attiya, Marc Snir, Manfred K. Warmuth
October 1988 **Journal of the ACM (JACM)**, Volume 35 Issue 4
Publisher: ACM Press

Full text available: pdf(2.27 MB) Additional Information: full citation, abstract, references, citings, index terms

The computational capabilities of a system of n indistinguishable (anonymous) processors arranged on a ring in the synchronous and asynchronous models of distributed computation are analyzed. A precise characterization of the functions that can be computed in this setting is given. It is shown that any of these functions can be computed in O(n2) messages in the asynchronous model. This is also proved to be a lower bound ...

16 On the sorting-complexity of suffix tree construction

Martin Farach-Colton, Paolo Ferragina, S. Muthukrishnan
November 2000 **Journal of the ACM (JACM)**, Volume 47 Issue 6
Publisher: ACM Press

Full text available: pdf(179.17 KB) Additional Information: full citation, abstract, references, citings, index terms

The suffix tree of a string is the fundamental data structure of combinatorial pattern matching. We present a recursive technique for building suffix trees that yields optimal algorithms in different computational models. Sorting is an inherent bottleneck in building suffix trees and our algorithms match the sorting lower bound. Specifically, we present the following results. (1) Weiner [1973], who introduced the data structure, gave an optimal 0 (n)-time al ...

Keywords: DAM model, RAM model, external-memory data structures, sorting complexity, suffix array, suffix tree

17 The circle-brush algorithm

K. C. Posch, W. D. Fellner
November 1988 **ACM Transactions on Graphics (TOG)**, Volume 8 Issue 1
Publisher: ACM Press

Full text available: pdf(1.46 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Brushing commonly refers to the drawing of curves with various line widths in hit-mapped graphics systems. It is best done with circles of suitable diameter so that a constant line width, independent of the curve's slope, is obtained. Allowing all possible integer diameters corresponding to all possible integer line widths results in every second width having an odd value. Thus, the underlying circle algorithm must be able to handle both integer and half-integer radii. Our ...

18 Structured programming

January 1972 Divisible Book
Publisher: Academic Press Ltd.

Full text available: pdf(11.44 MB) Additional Information: full citation, abstract, cited by, index terms

In recent years there has been an increasing interest in the art of computer programming, the conceptual tools available for the design of programs, and the prevention of programming oversights and error. The initial outstanding contribution to our

understanding of this subject was made by E. W. Dijkstra, whose Notes on Structured Programming form the first and major section of this book. They clearly expound the reflections of a brilliant programmer on the methods which he has hitherto uncon ...

19 Slowing sequential algorithms for obtaining fast distributed and parallel algorithms: maximum matchings

Baruch Shieber, Shlomo Moran

November 1986 **Proceedings of the fifth annual ACM symposium on Principles of distributed computing PODC '86**

Publisher: ACM Press

Full text available: pdf(790.52 KB) Additional Information: full citation, references, citings, index terms

20 Parallel Tridiagonal Equation Solvers

Harold S. Stone

December 1975 **ACM Transactions on Mathematical Software (TOMS)**, Volume 1 Issue 4

Publisher: ACM Press

Full text available: pdf(1.23 MB) Additional Information: full citation, references, citings, index terms

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next